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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/580,619	05/24/2006	Raymond J.E. Hueting	GB03 0213 US1	5566

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
09/08/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/580,619	HUETING ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1 to 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

Acknowledgement is made of papers filed claiming priority from Great Britain Patent Application No. 0327793.6 filed on November 29, 2003.

Information Disclosure Statement

To date no Ids has been filed in this case.

Drawings

New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because description paras 007, 0011 etc. describe the claimed (claim1 , etc.) the base of each trench is filled with an insulator plug adjacent to substantially all of the length of the drift region between the body region and drain region, however this recited element is not clearly numbered/ marked in the presently filed drawings.

Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 to 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujishima. (U.S. patent No. 5,981,996 herein after Fujishima) (also submitted by Applicants' in their IDS).

With respect to claim 1Fujishima describes an insulated gate field effect transistor, comprising:
a source region of first conductivity type (fig.1, 104) ; a body region of second conductivity type opposite to the first conductivity type adjacent to the source region (fig.1,111) ; a drift region of exclusively the first conductivity type adjacent to the body region (fig.1,102) ; a drain region of first conductivity type adjacent to the drift region, (fig.1, 109) so that body and drift regions are arranged between the source and drain regions (fig.1) , the drain region being of higher doping density than the drift region (col. 10 line 10 and inherent because drain region below drift and therefore higher doping density) ; and insulated trenches extending from the source region through the body region and into the drift region each trench having sidewalls and including insulator on the sidewalls (figs.1,4 105,insulator-406) , and a conductive gate electrode between the insulating sidewall, (fig. 1, 107) wherein the base of each trench is filled with an insulator plug adjacent to substantially all of the length of the drift region between the body region and drain region .(to the extent understood- fig. 1, 112) and the respective gate electrode is provided in the trench over the plug adjacent to the source and body (fig.1 107) .

*With respect to claim 2 Fujishima describes a*n insulated gate field effect transistor according to claim 1 wherein the doping concentration in the drift region is lower adjacent to the body region than adjacent to the drain region. (it is inherent that the portion of the drift region in figs. , e.g. fig.1 at a higher level i.e. adjacent drift region have lower doping concentration than the portion of the drift region at a lower level (adjacent to the drain region 109) .

*With respect to claim 3 Fujishima describes a*n insulated gate field effect transistor according to any preceding claim wherein the doping concentration in the body region is in the range of about 0.5x1017 cm3 to about 3 x 10 17 $cm^{-3,}$ and the doping concentration in the drift region) is in the range about 1 x l 015 cm^{-3} to about 2x l 017 $cm^{"3}$. (col. 8 lines 45,46-49,54; col. 9-55 ;10-5,10).

*With respect to claim 4 Fujishima describes a*n insulated gate field effect transistor according to claim 1 wherein the plug is of dielectric filler filling the trench between the insulator on the sidewalls adjacent to the drain region . (Fig. 1, 106).

With respect to claim 5 Fujishima describes an insulated gate field effect transistor according to claim 1 having a semiconductor body (fig.1, 111) having opposed first-(fig. 1) second major surfaces (fig. 1), wherein the source region (104) is at the first major surface over the region , the body region (111) is over the drift region (102) and the drift region (102) is over the drain region (109), and the trench (105)extends from the first major surface towards the second major surface through the source (104), body (111) and drift (102) regions.

*With respect to claim 6 Fujishima describes a*n insulated gate field effect transistor according to claim 5 having a plurality of cells each cell having a source region at centre of the cell surrounded by the insulated trench. (col. 12 line 61).

*With respect to claim 7 Fujishima describes a*n insulated gate field effect transistor according to claim 6 wherein the cells have a hexagonal geometry. (well known in the art e.g. Hark also cited by applicants in their IDS).

With respect to claim 8 Fujishima describes an insulated gate field effect transistor according to claim 6 wherein the trench (figs. 105) has gate oxide (Fig.106) on the sidewalls, and the of the trench adjacent to the drift region is filled with filler oxide between the gate oxide (fig. 112) on the sidewalls on either side of the trench. (fig.112).

*With respect to claim 9 Fujishima describes a*n insulated gate field effect transistor according to claim 5 having a plurality of cells (col. 12 line 61) arranged as stripes across the first major surface (Fig.1) with alternating trenches (105) and source regions (104).

With respect to claim10 Fujishima describes an insulated gate field effect transistor according to claim 6 wherein the cell pitch is in the range of about 0.2 microns to about 0.7 microns. (col. 9 lines 35 to col. 10 lines 19).

The prior art listed in the Pto-892 are included to show the state of the art in the IGFET transistor field.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN H. RAO whose telephone number is (571)272-1718. The examiner can normally be reached on 8.30-5.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Steven H Rao/
Examiner, Art Unit 2814

/Howard Weiss/
Primary Examiner, Art Unit 2814